Claims:

1. A method, comprising:

moving integrated circuit state into on-die storage and externally disabling power to on-die combinational circuitry.

2. The method of claim 1, wherein disabling power further includes tri-stating an output of a power supply regulator that provides power to the on-die combinational circuitry.

3. The method of claim 1, wherein disabling power further includes gating an off-die clamp to disrupt power supplied from an external power supply regulator to the on-die combinational circuitry.

4. The method of claim 1, wherein disabling power further includes gating an on-die clamp to disrupt power supplied from an external power supply regulator to the on-die combinational circuitry.

5. The method of claim 1, further including reapplying power after the integrated circuit receives an interrupt.

6. The method of claim 1, further including:

supplying the power from a power supply regulator along a path to the on-die combinational circuitry; and

providing a feedback signal from the path to the power supply regulator.

7. A method comprising:

forcing a high impedance state on an output of a power supply regulator that is coupled to a power pin of an integrated circuit.

8. The method of claim 7 wherein forcing a high impedance state further includes:

de-asserting a drive pin coupled to a gate of a MOS power transistor to force the high impedance state on the output of the power supply regulator.

9. The method of claim 8 further comprising:

connecting a diode to a source of the MOS power transistor.

10. The method of claim 7 further comprising:

timing the de-assertion to avoid high voltages on a supply inductor coupled between the output of the power supply regulator and the power pin of the integrated circuit.

11. A circuit comprising:

a first terminal of an integrated circuit coupled to receive power when the integrated circuit is in an active mode and not receive power when the integrated circuit is in a low power mode; and

a second terminal to receive power supplied to circuitry for low power state retention when the integrated circuit is in the low power mode.

12. The circuit of claim 11 further comprising:

a transistor external to the integrated circuit to gate the power received at the first terminal.

13. The circuit of claim 12, wherein the transistor is coupled to a power regulator and switched off when the integrated circuit is in the low power mode.

14. The circuit of claim 11 wherein a feedback signal is taken from the first terminal and supplied to a power regulator.

15. The circuit of claim 11 wherein a feedback signal is taken from within the integrated circuit and supplied to a power regulator.

16. The circuit of claim 11 further including a multiplexer to receive a signal taken from within the integrated circuit and a signal external to the integrated circuit, where an output of the multiplexer is coupled to a power regulator.

17. The circuit of claim 11 further comprising:

a transistor internal to the integrated circuit to gate the power received at the first terminal and float an internal power conductor connected to combinational logic.

18. A system comprising:

an integrated circuit having a power terminal coupled through an external control transistor to an output of a power supply.

19. The system of claim 18 wherein the control transistor is an NMOS transistor.

20. The system of claim 18 wherein the control transistor is a CMOS pass gate.

21. The system of claim 18 further including:

a multiplexer to couple a power signal supplied at a pin of the integrated circuit to the power supply while the integrated circuit operates in an active mode.

22. The system of claim 21 wherein the multiplexer disconnects the power signal from the power supply while the integrated circuit is in a low power standby mode.